Notice of Allowability	Application No.	Applicant(s)	
	09/712,130	BOWES, MICHAEL J.	
	Examiner	Art Unit	
	Michael J. Moore, Jr.	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7/13/2004*.

2. ☒ The allowed claim(s) is/are *1-5*.

3. ☒ The drawings filed on *26 March 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Allowable Subject Matter

1. Claims **1-5** are allowed.

2. The following is an examiner's statement of reasons for allowance:

Regarding claim **1**, the prior art of record teaches a network switch with an Internet port interface controller comprising a memory and a high performance interface. The prior art of record also teaches the transmission of data on both a rising edge and a falling edge of a clock signal. The prior art of record also teaches output drivers and a multiplexing circuit. The prior art of record also teaches the use of multiplexers for glitch reduction. The prior art of record fails to teach a multiplexing circuit that contains two levels of "glitchless" multiplexers used to serialize data.

Regarding claims **2-4**, these claims are further limiting to claim **1** and are thus also allowable over the prior art of record.

Regarding claim **5**, the prior art of record teaches a method of sending data through a high performance interface of a network switch. The prior art of record also teaches receiving parallel data over a high performance interface. The prior art of record also teaches the multiplexing of parallel data. The prior art of record also teaches the use of multiplexers for glitch reduction. The prior art of record also teaches hazards resulting from input state changes. The prior art of record fails to teach the storing of a portion of parallel data in a first register clocked on a positive edge of a clock signal. The prior art of record also fails to teach the storing of another portion of parallel data in a second register clocked on a negative edge of a clock signal. The prior art of record also fails to teach selecting alternating inputs to be multiplexed onto

the output of a second level "glitchless" multiplexer based upon the second level "glitchless" multiplexer selection signal. The prior art of record also fails to teach where the alternating input selection is timed so that the second level "glitchless" multiplexer only selects the input not producing a "function hazard".

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

3. Applicant's arguments, filed 7/13/2004, with respect to claims **1-5** have been fully considered and are persuasive. The rejections of claims **1-5** have been withdrawn.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Raghunathan et al. (U.S. 6,324,679) teaches a method for the reduction of power consumption in digital VLSI sequential circuits by reducing glitches in multiplexing circuits. This method makes use of multiplexer restructuring to reduce the propagation of glitches on data signals. Raghunathan et al. fails to teach the transmission of data on both a rising edge and a falling edge of a clock signal. Raghunathan et al. also fails to teach selecting alternating inputs to be multiplexed onto the output of a second level "glitchless" multiplexer based upon the second level "glitchless" multiplexer selection signal. Raghunathan et al. also fails to teach where the alternating input selection is

timed so that the second level "glitchless" multiplexer only selects the input not producing a "function hazard".

Segaram (U.S. 6,775,328) teaches a high-speed communication system with feedback synchronization that makes use of a gigabit serdes high-speed interface. Segaram fails to teach a multiplexing circuit that contains two levels of "glitchless" multiplexers used to serialize data. Segaram also fails to teach the same limitations lacking from the Raghunathan et al. reference.

Hayashi et al. (U.S. 6,556,583) teaches a transmitter and receiver circuit for data synchronization purposes that makes use of D latch circuits as well as a cascade of multiplexer circuits. Hayashi et al. fails to teach a multiplexing circuit that contains two levels of "glitchless" multiplexers used to serialize data. Hayashi et al. also fails to teach the same limitations lacking from both Raghunathan et al. as well as Segaram stated above.

Kosco (U.S. 5,793,236) teaches an integrated circuit that provides for doubled data throughput by clocking data on both the rising edge and falling edge of a clock signal. Kosco fails to teach a multiplexing circuit that contains two levels of "glitchless" multiplexers used to serialize data. Kosco also fails to teach the same limitations lacking from both Raghunathan et al., Segaram, and Hayashi et al. stated above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Moore, Jr. whose telephone number is (571) 272-3168. The examiner can normally be reached on Monday-Friday (8:30am - 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao can be reached at (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael J. Moore, Jr.
Examiner
Art Unit 2666

mjm MM

FRANK DUONG
PRIMARY EXAMINER